U.S. UTILITY Patent Application

APPL NUM	FILING DATE	CLASS	SUBCLASS	GAU	EXAMINER
10061475	02/01/2002	257		2811	Loke

APPLICANTS: Krutsick Thomas;

CONTINUING DATA VERIFIED:

none
Loke

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** FOREIGN APPLICATIONS VERIFIED:

none
Loke

PG-PUB	DO NOT PUBLISH ☐	RESCIND ☐	

Foreign priority claimed	☐ yes ☑ no	ATTORNEY DOCKET NO
35 USC 119 conditions met	☐ yes ☑ no	
Verified and Acknowledged Examiners's intials *Loke*		10

TITLE : Method of fabricating complementary self-aligned bipolar transistors

U.S.DEPT. OF COMM./PAT.& TM-PTO-436L(Rev. 12-94)

NOTICE OF ALLOWANCE MAILED		CLAIMS ALLOWED	
	Assistant Examiner	Total Claims	Print Claim for O.G
ISSUE FEE		DRAWING	
Amount Due Date Paid		Sheets Drwg. Figs.Drwg. Print Fig.	
	Primary Examiner		
☐ TERMINAL DISCLAMER	PREPARED FOR ISSUE	Application Examiner	

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